

Station and method for operating a CAN communication line

BACKGROUND OF THE INVENTION

The invention relates to a method for operating a low-speed CAN communication line using a flipflop-based CAN transceiver whilst detecting a ground level shift, according to the preamble of Claim 1. Background art referencing is provided by the ISO 11898 Specification Standard and the earlier art ISO 115 119 incorporated therein. Present day communication line systems need a reliable detection of an actual ground level, and as the case may be, of a shift in such ground level, to thereby correctly assess the actual binary information value and to ensure the proper operation of a bus failure management. Technically, it is possible to compare one line/bus level with the actual ground level, and to use the information so gathered for effecting the communication proper. Now, a too large or too small difference between the excitation signal and ground may indicate a particular ground shift. Such difference may be sampled repeatedly during operating the communication. It has been recognized that taking a single sample of the ground shift may be insufficiently reliable, and furthermore, that repeating such sampling will in many situations not improve that situation.

A further problem is presented by the fact that the line in question could be connected to various stations that operate according to individual non-uniform synchronizations. This may result in interference between the various stations, so that a transmitting station may detect a faulty ground shift caused by the various propagation delays that may play a part. In particular, during bus arbitration, various stations may start at mutually uncontrolled instants. The situation will even deteriorate when an acknowledge bit will signal a correct message reception at the receiver, because various slaves will not be synchronized.

SUMMARY TO THE INVENTION

In consequence, amongst other things, it is an object of the present invention to provide a method for reliably and inexpensively detecting a ground shift, which method can be guaranteed through a simple software routine. It has been found that often the cheapest solution is to use a single flipflop to store only the most recently sampled ground

shift value. The ground shift detection flipflop contains valid information only at the end of a message sent by the associated station. Such is true in any case after the arbitration has finished, because subsequently, no delay problems will exist anymore. A successful message transmission may cause generating a transmit interrupt signal.

5 Reference is had already to Figure 1, that will be discussed more in detail hereinafter. Now, a transmit interrupt signal may emanate from block 26. If the bus failure management in block 28 does not report a bus error, the above-mentioned software routine should read the ground shift flip flop before transmission of a next bit of the dominant value. Such dominant bit may be transmitted as acknowledging correct message reception or for
10 starting a next message.

 A particular further problem to be solved is the following. It may occur that after a transmitting CAN controller has signalled a transmit interrupt to the microcontroller, another connected CAN controller will put an error/overload flag on the same CAN bus. Such is conventionally effected through transmitting six dominant bits. In this case, the CAN
15 controller will automatically react with transmitting an error/overload flag on the CAN bus, also represented by six dominant bits. Such will not be reported by the microcontroller at the receiving end, but will be handled completely within the associated CAN controller, as it is a part of the standard CAN procedure. Now, to avoid overwriting of a ground shift sample, such sample will **not** be updated while the CAN transceiver is receiving dominant bits,
20 RxD=0. Also the handling of the above-sketched problem situation is an object of the present invention.

 Now therefore, according to one of its aspects the invention is characterized according to the characterizing part of Claim 1.

 The invention also relates to a station, a station-and-line system, and a multi-
25 device system arranged for implementing the invention as claimed in Claims 6, 7 and 8, respectively. Further advantageous aspects of the invention are recited in dependent Claims.

BRIEF DESCRIPTION OF THE DRAWING

 These and further aspects and advantages of the invention will be discussed
30 more in detail hereinafter with reference to the disclosure of preferred embodiments, and in particular with reference to the appended Figures that show:

 Figure 1, a block diagram of a station/node arrangement according to the invention;

Figure 2, functional principal electronic circuitry for implementing the invention;

Figure 3, an exemplary frame format of a CAN bus for implementing the invention;

5 Figure 4, a CAN bus signal trace arrangement generated by the low-speed CAN transceiver according to the invention;

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 illustrates by way of non-limiting example a block diagram of an arrangement according to the invention, and in particular for use with the Controller Area Network or CAN that is based on two parallel bus lines CAN_H(igh) 20 and CAN_L(ow) 22. Both bus lines attach to the single station that has been illustrated by way of example, but which may represent various stations in parallel. The station has three hierarchically organized subsystems 24, 26, 28. The highest layer is microcontroller 24 that can execute user and/or system software and will communicate with the next lower level through appropriate signalization patterns. Note that the transmit interrupt from block 26 will trigger the software routine for reading the ground shift flag in block 28.

The second layer is CAN controller 26, which is arranged for formatting and communicating system and user data for use on the net or bus, and for implementing an appropriate bus protocol, inclusive of deciding the direction of such communicating, and the associated addressing, packaging and possibly error protection features. The vehicle for the communicating is the TX0/RX0 signal pair as indicated, that on the transceiver is represented by the TxD and RxD signal pair, respectively.

The third level is CAN transceiver 28, which is arranged for effecting the lowest level communication aspects, inclusive of the generating of the CAN bus signals CAN_H and CAN_L as indicated.

Figure 2 illustrates electronic circuitry for implementing the invention. One of the two bus lines, here CAN_H 30, and overall ground are fed into an accurate comparator 34 as shown. This comparator will output a logic "1" if $(CAN_H - GND) < -1,2$ volts. Generally, tolerances for this threshold value are in the region of 320%. On the other hand, this comparator will output a logic "0" if $(CAN_H - GND) > -1,2$ volts. Note that corresponding values will apply when operating on the other signalling level. The output signal is fed into the "1" input of multiplexer 40, that is controlled by a representation of the RxD signal received in transceiver module 28 in Figure 1. The output of multiplexer 36 feeds the data or

“D” input of flipflop 40 that loads under control of a rising-edge of the signal from inverter 46. The inverter inverts a signal TXD received on input 44. Output 42 therefore carries a ground shift sample bit that is retrocoupled to the 0 input of multiplexer 36, so that the stored bit is kept persistent, in the case of an overload frame.

5 Figure 3 illustrates an exemplary data frame format of a CAN bus as a non-limiting vehicle for implementing the invention. Following an interframe space a control field, a data field, a CRC check sum field, an ACKnowledge field, and an end-of-frame signalization. The next interframe space allows an overload frame if relevant.

Figure 4 illustrates CAN bus signal traces as generated in the embodiment.

10 Reference is had to the subsystem arrangement of Figure 1. The top trace is the output from controller 26, which drives transitions on the complementary bus lines (28), from 5 to 1.4, and from 0 to 3.6 volts, respectively. The next trace is the differential that goes from -5 volts to +2.2 volts, and whereof a -3.2 threshold level the V_RXD that actuates multiplexer 36 in Figure 2. Shown in particular are the delay between the edges of V_TXD and the V_RXD
15 reaching its new level.

PHNL000425-0744